

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
Sadami Takeoka et al.) Group Art Unit: Unknown
Serial No.:)
(Continuation of Serial No. 08/803,145))
Filed: April 30, 2001)
Title: METHOD OF DESIGNING SEMI-) Examiner: THAI PHAN
CONDUCTOR INTEGRATED CIRCUIT)

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 3, 4, 6, 7, 9, 10, 13, 14, and 18 without prejudice or disclaimer.

Please amend claims 1, 2, 5, 8, 11, 12, 15, 17, 19 and 20 as follows:

1. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor

integrated circuit] comprising:

a first step of selecting [connecting] one output terminal out of plural output terminals of a first memory element; and

a second step of connecting the selected output terminal of the first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein both said first step and said second step are performed on the basis of physical layout information.

2. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating a beeline distance on a substrate from each of said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum beeline distance to said scan data input terminal of said second memory element with said scan data input terminal of said second memory element.

5. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating wire lengths to be laid from said output terminals of said first memory element to said scan data input terminal of said second memory element; and

connecting one of said output terminals of said first memory element having a minimum wire length with said scan data input terminal of said second memory element.

8. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes steps of:

calculating fan-out of said output terminals of said first memory element;
and

connecting one of aid output terminals having minimum fan-out with said scan data input terminal of said second memory element.

11. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

a first step of selecting [connecting] one output terminal out of plural output terminals of a first memory element; and

a second step of connecting the selected output terminal of the first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein both said first step and said second step are performed on the basis of physical timing information.

12. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a

scan test function,

wherein said element connecting step includes steps of:

calculating load capacitances of said output terminals of said first memory element; and

connecting one of said output terminals of said first memory element having a minimum load capacitance with said scan data input terminal of said second memory element.

15. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having a maximum driving ability and connecting said selected output terminal with said scan data input terminal of said second memory element.

17. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor

integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

connecting one of said output terminals of said first memory element having a design margin larger than a predetermined value with said scan data input terminal of said second memory element, said design margin being obtained as a difference between one cycle time of a clock signal and propagation time required for a signal to travel from each of said output terminals of said first memory element to another memory element or an external output port.

19. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first memory element having maximum delay time of a signal received at said scan data input terminal of said first memory element and connecting said selected output terminal with said scan data input

terminal of said second memory element.

20. (Amended) A method of wiring a semiconductor integrated circuit to include a scan chain between first and second memory elements previously selected in the semiconductor integrated circuit, said method [A method of designing a semiconductor integrated circuit] comprising:

an element connecting step of connecting one of plural output terminals of a first memory element having a scan data input terminal with a scan data input terminal of a second memory element having a scan test function,

wherein said element connecting step includes a step of:

selecting one of said output terminals of said first element having delay time of a signal received at said scan data input terminal of said first memory element larger than a predetermined value and connecting said selected output terminal with said scan data input terminal of said second memory element.

REMARKS

The present application is a continuation of U.S. Serial No.: 08/803,145, in which claims 3, 4, 6, 7, 9, 10, 13, 14 and 18 stand allowed at the time of this preliminary amendment. Claims 1, 2, 5, 8, 11, 12, 15-17, 19 and 20 are pending in the present application. These claims, as amended, are considered to be allowable over the prior art of record.

If there are any outstanding issues that might be resolved by an interview or an

Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Dated: April 30, 2001

By:



Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, D.C. 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087
WDC99 427017-1.043889.0937